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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,124	KAWAGUCHI, KENICHI	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) *11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/03/2008 has been entered.

RESPONSE TO ARGUMENTS

2. Applicant's arguments filed 06/03/2008 have been fully considered but they are not persuasive. Previous rejection of claims 2-8 under 35 U.S.C. 112 second paragraph is withdrawn. Currently, claims 1 and 9-10 are canceled, claim 11 is withdrawn, and claims 2-8 and 12 are pending for examination

3. In response to applicant's arguments (on page 9) regarding to the amended independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest M > 2 because Kato's teaching of the jump start address and jump end address provides M=1; applicant's arguments have fully been considered, but are not found to be persuasive.

In combination with the examiner's assumption below that the operation is repeated for M – 1 time; the examiner respectfully disagrees, as the combination of the references expressly teaches wherein M > 1 (e.g. 2 data words to be transferred) with the operation being repeated for M - 1 (e.g. 1) times , it would have been an obvious design choice to implement M > 2 for the DMA burst transferring by including more then 2 data words (e.g. M = 3 data words) for transferring that have more than 1 jump (e.g. 2 jump) while transferring (i.e. operation is repeated M – 1 = 2 times), wherein Kato's teaching can accommodate such implementation by initializing Kato's DMA burst transfer to have a plurality of jump start addresses stored in the jump start address register (Fig. 1, ref. 16) and a plurality of jump end addresses stored in the jump end address register (Fig. 1, ref. 18) (Kato, col. 1, ll. 47-67 and col. 3, l. 12 to col. 4, l. 25); additionally, it is well known in the art for the DMA burst transferring to include more then 2 data words (Tang, col. 3, ll. 36-42).

I. REJECTIONS BASED 35 U.S.C. 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-8 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 2 and 12, in view of applicant's explanation with regard to the claimed limitation "M" in applicant's remarks on page 9, it appears that if "M"

is the number of words to be transferred, then the operation should be repeated "M-1" times, rather then "M" times, and vice versa (e.g. if "M" is the number of repetition, then "M+1" is the number of words to be transferred); the examiner will assume the claimed limitation of "... the operation is repeated for M-1(2<M) times periodically ..." for each respective amended independent claims 2 and 12 for the current examination.

As per claims 3-8, dependent claims 3-8 are also rejected at least due to direct/indirect dependency on the rejected independent claim 2.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717).

AAPA teaches a data transfer control system and method connected to a bus for controlling a data transfer to a device on the bus, comprising:

a data storing step (Drawings, data register 143 of Fig. 19) comprising means for storing data (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7);

a transferred-word number storing step (Drawings, transferred-word number register 103 of Fig. 19) comprising means for storing the number of words of data which are to be transferred (Specification, page 1, l. 9 to page 2, l. 7);

a bus cycle controlling step (Drawings, cycle control section 105 of Fig. 19) comprising means for controlling the data transfer such that, during a burst transfer, in a single bus cycle, a write control line (byte enable register of Fig. 20A-20B) of the bus is placed in a write-enabled state (i.e. byte enable register set to "0000") for a one word-data transfer period (i.e. period during the transferring of "Data1") and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state (Specification, page 1, l. 9 to page 2, l. 7);

wherein M is the number of words of data which are to be transferred and stored in the transferred-word number storing means, and M > 1 as there are at least Data 1 and Data 2 to be transferred (Drawings, transferred-word number register 103 of Fig. 19 and Specification, page 1, l. 9 to page 2, l. 7); and

wherein the destination addresses (e.g. addresses "4000000" and "4000008"), to which the plurality of one world data (e.g. "Data1" and "Data2")

included in the data are to be transferred, are equally spaced (e.g. "000004" bytes) (Fig. 20A-20B).

AAPA does not teach the data transfer control system and method connected to the bus for controlling the data transfer to the device on the bus comprising:

a transfer interval storing step of storing an interval between data destination addresses, equally separating the addresses;

the bus cycle controlling step, during the single bus cycle, the bus is driven continuously and the write control line is place in a write-disable stated for (N-1) word period and the operation is repeated for M times periodically, wherein N is the number store in the transfer interval storing step; and

wherein $M > 2$.

Kato teaches a direct memory access (DMA) data transferring system and method comprising:

a transfer interval storing step of storing an interval between data destination addresses, equally separating the addresses (col. 3, ll. 12-15 and col. 3, l. 53 to col. 4, l. 25), wherein the combination of a jump start address register (Fig. 1, ref. 16) and a jump end address register (Fig. 1, ref. 18), initialized by a CPU (Fig. 1, ref. 300), stores the intervals which provide when data are to be transferred or not to be transferred; and

the bus cycle controlling step (e.g. control associated with DMA controller 100 of Fig. 1 having the read/write controller 14 of Fig. 1), during the single bus cycle, the bus is driven continuously (e.g. does not require re-initialization of the

DMA controller) and the write control line is place in a write-disable stated for (N-1) word period and the operation (e.g. read/wrote) is repeated for M times periodically, wherein N is the number store in the transfer interval storing step (col. 1, ll. 47-67 and col. 3, l. 43 to col. 4, l. 25), as the read/write controller enables and disables the write control line periodically, such that the write control line is enabled during the data transferring intervals and disabled during the non-data transferring intervals as indicated by the jump start address register and the jump end address register, wherein the jump start address register and the jump end address register would store the corresponding transfer interval; therefore, during the single burst of data transfer, when memory areas exist that is not to be read/write, those areas would be bypassed (jumped) periodically ; and

furthermore, as the combination of the references expressly teaches wherein M > 1 (e.g. 2 data words to be transferred) with the operation being repeated for M - 1 (e.g. 1) times, it would have been an obvious design choice to implement M > 2 for the DMA burst transferring by including more then 2 data words (e.g. M = 3 data words) for transferring that have more than 1 jump (e.g. 2 jump) while transferring (i.e. operation is repeated M – 1 = 2 times), wherein Kato's teaching can accommodate such implementation by initializing Kato's DMA burst transfer to have a plurality of jump start addresses stored in the jump start address register (Fig. 1, ref. 16) and a plurality of jump end addresses stored in the jump end address register (Fig. 1, ref. 18) (col. 1, ll. 47-67 and col. 3, l. 12 to col. 4, l. 25); additionally, it is well known in the art for the DMA burst transferring to include more then 2 data words (Tang, col. 3, ll. 36-42).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kato's DMA controller into AAPA's data transfer control system and method for the benefit of optimize the efficiency of data transferring by enabling the large amount of data transferring without the intervention of the CPU (Kato, col. 1, ll. 47-59 and col. 3, ll. 49-52) to obtain the invention as specified in claims 2 and 12.

6. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717) as applied to claim 2 above, and further in view of Sheafor et al. (US Patent 6,321,285) and Kreifels (US Patent 4,891,788).

7. As per claim 3, AAPA and Kato teach all the limitations of claim 2 as discussed above, where AAPA further teaches the data transfer control system comprising:

cycle start address storing (AAPA, Drawings, cycle start address register 108 of Fig. 19) means for storing a start address of a bus cycle (AAPA, Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7); and

interrupted-cycle resuming (AAPA, Drawings, interrupted-cycle resuming section 105c of Fig. 19).

AAPA and Kato does not expressly teach the data transfer control system further comprising:

resumption address calculating means for calculating a destination address of second data ...; and

means for transferring the address calculated by the resumption address calculating means to the cycle start address storing means to start a new bus cycle ... .

Sheafor teaches a data transfer control system comprising the interruption of the connection between the master device and the slave device, as the master device detect and thus informed by the slave device of said interruption, the master device then restart transfer of next set of data with a new address (col. 38, l. 34 to col. 40, l. 32), wherein the derivation of the new address would obvious require calculation.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Sheafor's new address upon initiation of the interrupt by the slave device into AAPA and Kato's data transfer control system for the benefit of proper transfer of data between master device and slave device upon detection of the interrupt in the connection initiated by either the master device or the slave device (Sheafor, col. 38, l. 34 to col. 40, l. 32) to obtain the invention as specified in claim 3. The resulting combination of the references teaches the data transfer control system further comprising upon detection of the interrupt while data transferring between the master device and the slave device, wherein the master device detect and thus informed by the slave device of said interrupt, the master device then calculate the new address and restart transfer

of next set of data with the new address; and the new address would have been transferred to the cycle start address storing means as the cycle start address storing means provides the start address for the new bus cycle.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA, Kato and Sheafor's data transferring control system for the benefit of providing a truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24) to obtain the invention as specified in claim 3. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

8. As per claim 7, AAPA, Kato, Sheafor and Kreifels teaches all the limitations of claim 3 as discussed above, where AAPA and Kreifels further teach the data transfer control system further comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transferring from data buffer to data register on Fig. 20A) when the write control line is in the write-disabled state (Kreifels, Fig. 1 and

col. 1, ll. 15-24), wherein write operation is enabled while the read operation is disabled by the write-disable stated, as data are not read out to be written.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717) as applied to claim 2 above, and further in view of Fabre (US Patent 6,993,605).

AAPA and Kato teach all the limitations of claim 2 as discussed above, where AAPA further teaches the data transfer control system further comprising wherein the data transfer conform to the PCI standard (AAPA, Drawings, Fig. 19), it would have been obvious that data can be transfer in a plurality of modes comprising burst mode and repeat transfer of a single word data mode.

AAPA and Kato does note expressly teach the data transfer control system further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode ...; and

transfer mode selecting means for selecting the burst transfer mode ... .

Fabre teaches a data transfer control system comprising:

a table (Fig. 2, ref. 170) storing information comprising a plurality of aggregate data transfer rates and corresponding data samples, wherein said information is characterized by the time delay between data transferred and

reception of response from the peripheral device (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42);

a optimizer (Fig. 2, ref. 180) comprising a comparator, base on the information stored in said table, determining the best and/or preferred aggregated data transfer rate (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42); and

selecting data sample to be use as model for future transfer (Fig. 2, ref. 185), wherein the selection would allow the specific peripheral to function at peak speed and efficiency (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fabre's table, optimizer and selection of data sample for future transfer into AAPA and Kato's data transfer control system comprising plurality of modes of data transferring for the benefit of providing the peak speed and efficient rate of data transferring between the CPU (master device) and the peripheral (slave device) (Fabre, col. 7, ll. 16-58) to obtain the invention as specified in claim 4.

10. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717) and further in view of Sheafor et al. (US Patent 6,321,285) and Kreifels (US Patent 4,891,788) as applied to claim 3, and further in view of Fabre (US Patent 6,993,605).

AAPA, Kato, Sheafor and Kreifels teaches all the limitations of claim 3 as discussed above, where AAPA further teaches the data transfer control system comprising wherein the data transfer conform to the PCI standard (AAPA, Drawings, Fig. 19), it would have been obvious that data can be transfer in a plurality of modes comprising burst mode and repeat transfer of a single word data.

AAPA, Kato, Sheafor and Kreifels does note expressly teach the data transfer control system further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode …; and

transfer mode selecting means for selecting the burst transfer mode ….

Fabre teaches a data transfer control system comprising:

a table (Fig. 2, ref. 170) storing information comprising a plurality of aggregate data transfer rates and corresponding data samples, wherein said information is characterized by the time delay between data transferred and reception of response from the peripheral device (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42);

a optimizer (Fig. 2, ref. 180) comprising a comparator, base on the information stored in said table, determining the best and/or preferred aggregated data transfer rate (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42); and

selecting data sample to be use as model for future transfer (Fig. 2, ref. 185), wherein the selection would allow the specific peripheral to function at peak speed and efficiency (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fabre's table, optimizer and selection of data sample for future transfer into AAPA, Kato, Sheafor and Kreifels' data transfer control system comprising plurality of modes of data transferring for the benefit of providing the peak speed and efficient rate of data transferring between the CPU (master device) and the peripheral (slave device) (Fabre, col. 7, ll. 16-58) to obtain the invention as specified in claim 5.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717) as applied to claim 2 above, and further in view of Kreifels (US Patent 4,891,788).

AAPA and Kato teach all the limitations of claim 2 as discussed above, where AAPA further teaches the data transfer control system further comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transfer to Data register on Fig. 20A) when the write control line is in the write-enabled state (AAPA, Drawings, write enabled when the byte enable register set to "0000") (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA and Kato does not teach the data transfer control system further comprising the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA and Kato's data transferring control system for the benefit of providing an truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24) to obtain the invention as specified in claim 6. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kato (US Patent 5,333,290) with additional support by Tang et al. (US Patent 6,775,717) and further in view of Fabre (US Patent 6,993,605) as applied to claim 4 above, and further in view of Kreifels (US Patent 4,891,788).

AAPA, Kato and Fabre teach all the limitations of claim 4 as discussed above, where AAPA further teaches the data transfer control system further

comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transferring from data buffer to data register on Fig. 20A) when the write control line is in the write-enabled state (AAPA, Drawings, write enabled when the byte enable register set to "0000") (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA, Kato and Fabre does not teach the data transfer control system further comprising the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA, Kato and Fabre's data transferring control system for the benefit of providing an truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24) to obtain the invention as specified in claim 8. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

III. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 2-8 and 12 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

July 23, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181